Experiment 9
MOS Transistor

In-Lab Report

MOSFET As Voltage-Controlled Resistor

Table 1.

$V_{GS} - V_T$ (Volts)	V_{DS}(Volt)	I_D (mA)
2	0.1	5.86
2	0.15	8.35
2	0.2	11.45
2	0.25	13.79
2	0.3	16.53
3	0.1	5.95
3	0.15	9.20
3	0.2	12.09
3	0.25	14.94
3	0.3	17.67
4	0.1	6.31
4	0.15	9.02
4	0.2	12.95
4	0.25	15.16
4	0.3	18.5

MOSFET Logic Gate

Table 2.

In-1 (Logic)	In-2 (Logic)	Out (Logic)	V$_{IN1}$ (Volts)	V$_{IN2}$ (Volts)	V$_{out}$ (Volts)
0	0	1	0.00	0.00	5.07V
0	1	0	0.00	5.00V	66.02mV
1	0	0	5.00V	0.00	66mV
1	1	0	5.00v	5.00v	20mv

Table 3.

V$_{IN1}$ (Volts)	V$_{out}$ (Volt)	MOSFET Region of Opration	Logical Value at output
0	5.06	cutoff	1
0.4	5.06	cutoff	1
0.8	5.06	cutoff	1
1.2	5.06	cutoff	1
1.6	5.06	cutoff	1
2.0	4.8	saturation	1
2.4	0.43	ohmic	0
2.8	90 mv	ohmic	0
3.2	80 mv	ohmic	0
3.6	78 mv	ohmic	0
4.0	76 mv	ohmic	0
4.4	75 mv	ohmic	0
4.8	73 mv	ohmic	0